Signal Conditioning Circuit Development

Addressing the Physical Limitation of Propagation Delays in Digital Control of Power Supplies

Kejdi R. Sulaj, Mitsi Dabbieri, Hani Alghazwi, Mamadou Djigo

Faculty Advisor: Dr. Zhiqiang Gao, Dr. Pong Chu

Department of Electrical Engineering and Computer Science, Cleveland State University

Problem Statement

The motivation behind this poster is to show a point by point description of the Signal Conditioning Circuit's propagation delay. It will clarify the reason and elements of the circuit, the constraints under which it must work, research and possible solutions about obtaining optimum results. A signal conditioning circuit is a device that converts one type of electronic signal into another type of signal. Its primary use is to convert a signal that may be difficult to read by conventional instrumentation into a more easily read format. The propagation delay of this circuit is an important factor on how fast the circuit can work, When one block of the circuit has a high delay, all the rest of the circuit will have to wait for this one block to provide a valid output.

- **Minimize propagation delay between 10ns- 100ns**
- **Isolation of front end signal**
- **Design schematics for SCC**

Design Specifications

As shown in Figure 1, this feedback loop allows for the analog signal to be processed through ADC, be isolated, and then be fed to an FPGA. This signal will be going to an isolated driver, then finally converted back to analog and fed back to the DC-DC power supply. Four investigation points and some of the challenges that come with this feedback loop design are listed

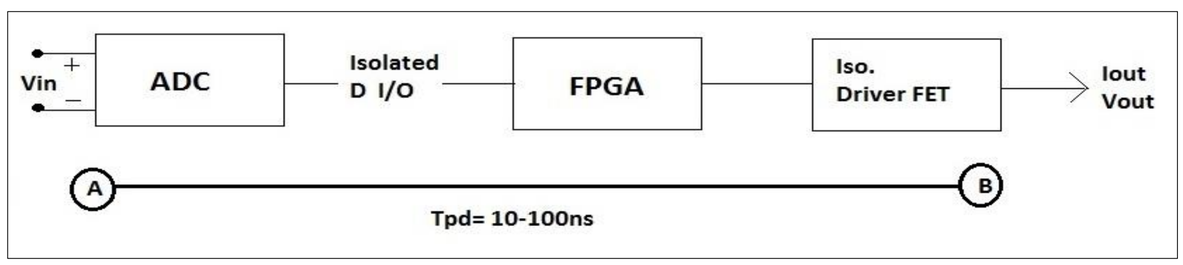


Figure 1: Signal Conditioning Circuit Feedback Loop

Front End Circuit Design

This front-end design is consisted of a voltage division to step down the input voltage at 4 volts and then fed to the first op-amp, which using a negative feedback loop is able to isolate the signal.. Once the signal passes the first op-amp, it then feeds to the bipolar op amp. This bipolar op amp has a negative feedback, connected to a reference input voltage of 15 volts followed by a 51k resistor. This step up will help separate the input 4 volts signal into +2 volts and -2 volts on the output side. This separation of the unipolar to bipolar output signal is crucial to the input of the ADC to make sure that no voltage is lost throughout the process.

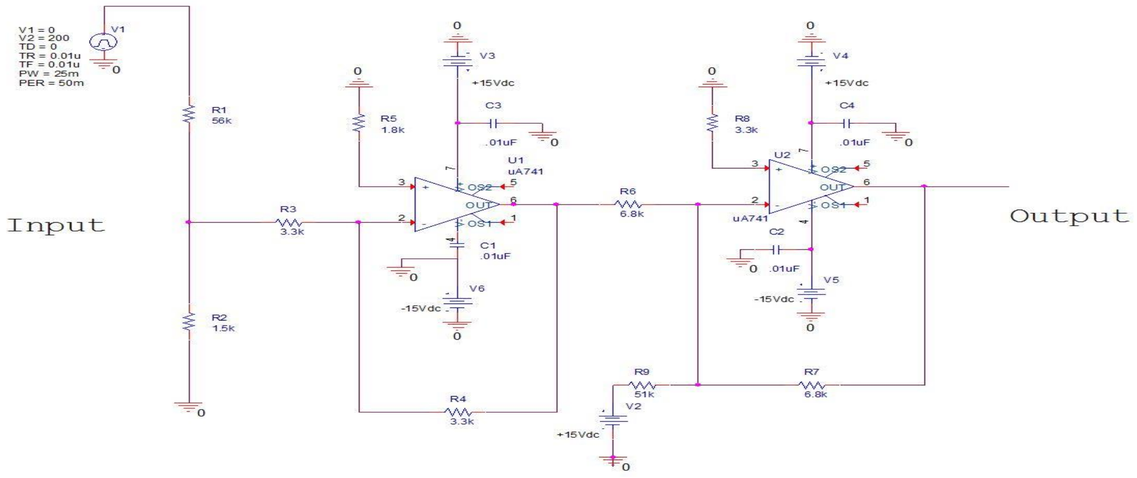


Figure 2: Circuit Design

Front End Circuit Testing and Simulations

In figure 3, is shown the tested and measured propagation delay of the front end circuit. The yellow signal represents the input signal and the green signal represents the output signal of the circuit. The propagation delay is measured between the input rising edge and output rising edge, and that difference is recorded at 14ns.

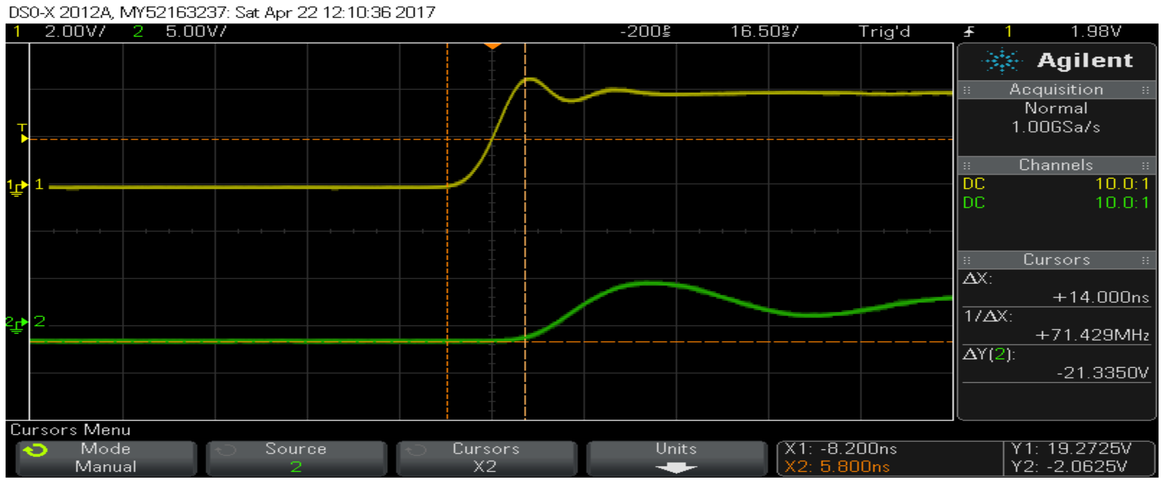


Figure 3: Simulation & Propagation Delay for Front End Circuit

FPGA Role in SCC

FPGA acts as a feedback control loop of the signal conditional circuit for almost pure signal without any distortion or noise. The FPGA implementation within the Signal conditioning circuit was done using hardware description languages (VHDL). FPGA has two main implemented side-by-side for signal conditioning: proportional integral derivative (PID) and pulse width modulator (PWM).

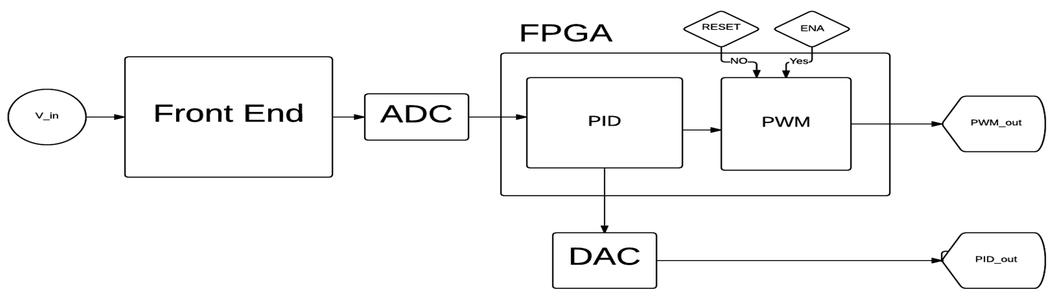
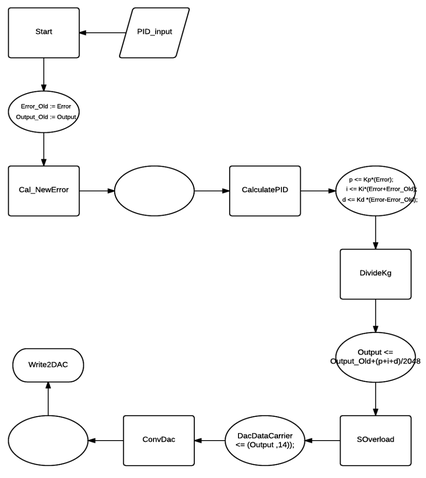


Figure 4: FPGA Topology

PID Logic In The Circuit

PID takes a 14 bit ADC output from the front end the SCC as input Using finite state Machine with data path (FSMD) the digital signal is conditioned Seven state with no condition to decide the next state but simply passing the data along the state (Start, CalculateNewError, CalculatePID, DivideKg, Write2DAC, SOverload, ConvDac)



Devices and Software

- Quartus 13.1 (simulation and testing)
- Signal Tap II analyzer is used for verification of the design and timing analysis
- Cyclone V GX 5CGXFC5C6F27C7N
- ADA daughter board are connected to the HSMC connector.
- Dual AD channels & SPI Interface